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WORKED EXAMPLES

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PART 1—Electrical and Electronic Principles IV (BTEC)

Q1 The circuit in Figure 1 represents a signal generator of EMF 4·5 V connected to a load resistor of 600 Ω. The internal impedance of the generator consists of an inductor of reactance 500 Ω in parallel with a 500 Ω resistor.

Obtain the Thévenin equivalent circuit of the generator and hence find the terminal voltage when the load is connected.

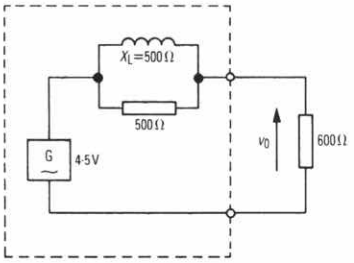


Figure 1

A1 When the load is removed, no voltage division takes place, so that the terminal voltage $v_{TH} = 4{\cdot}5$ V.

The Thévenin impedance, Z_{TH}, when the generator is replaced by a short circuit is the parallel value of X and R. Using product over sum to find Z_{TH},

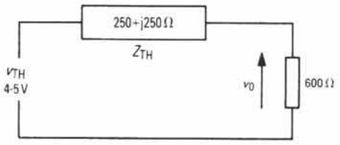
$$Z_{TH} = \frac{500 \times j500}{500 + j500} = \frac{j500}{1 + j1}.$$

Rationalising,

$$Z_{TH} = \frac{j500(1 - j1)}{1^2 + 1^2} = \frac{500 + j500}{2}.$$

$$\therefore \quad Z_{TH} = 250 + j250\,\Omega.$$

The circuit now becomes



The terminal voltage can now be obtained by voltage division:

$$v_0 = 4{\cdot}5\frac{600}{600 + 250 + j250}\ \text{V},$$

$$= \frac{4{\cdot}5 \times 600}{850 + j250},$$

$$= \frac{4{\cdot}5 \times 6}{8{\cdot}5 + j2{\cdot}5}.$$

$$\therefore \quad |v_0| = \frac{4{\cdot}5 \times 6}{\sqrt{(8{\cdot}5^2 + 2{\cdot}5^2)}} = \underline{3{\cdot}047\ \text{V}.}$$

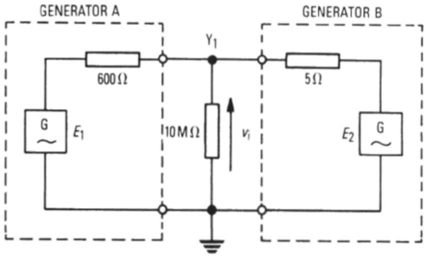
> The great advantage of the use of the Thévenin Equivalent circuit is that a quick solution is possible when the load value is changed. Other methods would require the problem to be started again from the beginning.

Q2 *In order to demonstrate the effect of second harmonic distortion on a waveform, the only two available signal generators are connected together and then connected to an oscilloscope of 10 MΩ input impedance.*

Generator A has an output impedance of 600 Ω and is set at an open circuit peak voltage of 2 V, 1000 Hz. Generator B has an output impedance of 5 Ω and is set at an open circuit peak voltage of 0·3 V, 2000 Hz.

(a) Draw the equivalent circuit of the arrangement.
(b) Using the superposition theorem, obtain an expression for the voltage which appears at the input terminals of the oscilloscope.
(c) Comment on the result obtained in (b).

A2 (*a*)



(*b*) For E_1

$$E_{\max} = 2\text{ V}; \qquad \omega = 2\pi f = 2\pi \times 1000 = 2000\pi\text{ rad/s}.$$

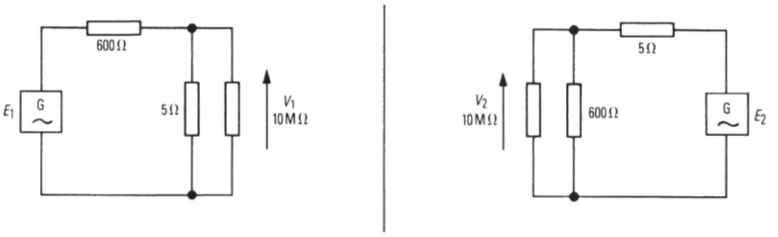
$$\therefore \quad E_1 = 2\sin 2000\pi t\text{ volts}.$$

For E_2

$$E_{\max} = 0{\cdot}3\text{ V}; \qquad \omega = 2\pi f = 2\pi \times 2000 = 4000\pi\text{ rad/s}.$$

$$\therefore \quad E_2 = 0{\cdot}3\sin 4000\pi t\text{ volts}.$$

The circuit is now separated into its two sections:



Since the loading effect of the 10 MΩ impedance is negligible, the parallel sections can be taken as 5 Ω and 600 Ω, respectively.

$$\therefore \quad V_1 = E_1\frac{5}{5+600},$$

$$= (2\sin 2000\pi t)\frac{5}{605},$$

$$= 0{\cdot}0165\sin 2000\pi t\text{ volts}.$$

$$\therefore \quad V_2 = E_2\frac{600}{600+5},$$

$$= (0{\cdot}3\sin 4000\pi t)\frac{600}{605},$$

$$= 0{\cdot}298\sin 4000\pi t\text{ volts}.$$

Combining these results,

$$v_i = V_1 + V_2,$$

$$= \underline{0{\cdot}0165\sin 2000\pi t + 0{\cdot}298\sin 4000\pi t\text{ volts.}}$$

(*c*) The result shows that the majority of the fundamental voltage is lost and therefore the displayed waveform will not appear as a sine wave distorted by a second harmonic component.

> This problem shows that generators of differing output impedances should not be connected directly together. The difficulty can be overcome by inserting a summing network whose resistances are much larger than the generator impedances. A typical network is shown.
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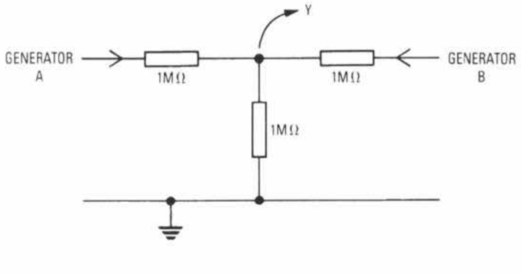
> 
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>
> The potential difference at Y will be approximately $\frac{1}{3}E_1 + \frac{1}{3}E_2$.

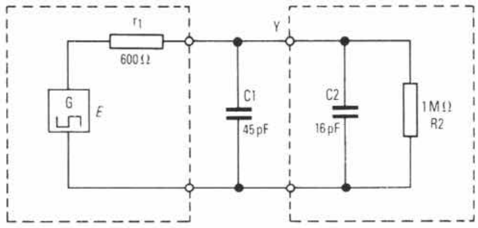
Q3 A signal generator of output resistance 600 Ω generates an ideal square wave. In order to examine the waveform, the signal generator is connected to the Y input of an oscilloscope via a coaxial cable. The coaxial cable has a capacitance of 45 pF between the inner and outer conductors. The input impedance of the Y input consists of a 1 MΩ resistance in parallel with 16 pF. Assume that the Y amplifier is loss free.

(*a*) *Draw the equivalent circuit.*

(*b*) *Calculate the rise time of the displayed waveform.*

(*c*) *What peak-to-peak open-circuit voltage is required from the generator to obtain 5 V peak-to-peak at the Y input?*

A3 (*a*)



(*b*)

> The rise time is given by
>
> $$t_r = 2{\cdot}2CR \text{ seconds,}$$
>
> where R is the effective series resistance and C the shunt capacitance. To use this formula, the circuit must be converted from a series/parallel arrangement to a series network. This may be achieved by the use of Thévenin's theorem. The capacitance is treated as the load.

Removing the capacitors, the Thévenin voltage is given by

$$V_{TH} = E\frac{R_2}{r_1 + R_2},$$

$$= E\frac{1 \times 10^6}{600 + (1 \times 10^6)},$$

$$= 0{\cdot}9994E \text{ volts.}$$

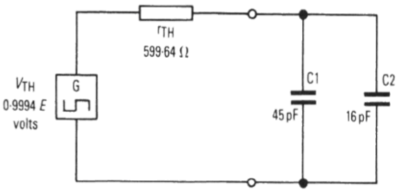
The Thévenin resistance, looking back towards the generator, is seen to be r_1 in parallel with R_2.

$$\therefore \quad \frac{1}{r_{TH}} = \frac{1}{r_1} + \frac{1}{R_2},$$

$$= \frac{1}{600} + \frac{1}{1 \times 10^6},$$

$$\therefore \quad r_{\mathrm{TH}} = 599{\cdot}64\,\Omega.$$

The Thévenin equivalent circuit is shown in the sketch.



From the equivalent circuit,

$$\begin{aligned} t_r &= 2{\cdot}2CR \text{ seconds,} \\ &= 2{\cdot}2(C_1 + C_2)599{\cdot}64 \text{ s,} \\ &= 2{\cdot}2 \times 61 \times 10^{-12} \times 599{\cdot}64 \text{ s,} \\ &= \underline{80{\cdot}47 \text{ ns.}} \end{aligned}$$

(*c*) For an input of 5 V peak-to-peak to the Y terminal, V_{TH} must be 5 V peak-to-peak.

$$V_{\mathrm{TH}} = 0{\cdot}9994E.$$

$$\begin{aligned} \therefore \quad E &= \frac{V_{\mathrm{TH}}}{0{\cdot}9994}, \\ &= \frac{5}{0{\cdot}9994} \text{ V,} \\ &= \underline{5{\cdot}003 \text{ V peak-to-peak.}} \end{aligned}$$

These results show that the voltage loss caused by the internal resistance of the generator is insignificant. However, the rise time is comparatively slow, and the oscilloscope and its coaxial cable would be quite unsatisfactory for use in the measurement of a high-frequency square wave. The ideal square wave becomes degraded when the coaxial lead is connected. When examining high-frequency waveforms such as experienced in digital systems an attenuator probe and wideband oscilloscope must be used.

Q4 *Figure 2 represents the circuit of an attenuator probe used in combination with a wideband oscilloscope for the examination of digital waveforms. The attenuation is a factor of 10 and, when capacitor C1 is set to its correct value, the waveform degradation is at a minimum.*

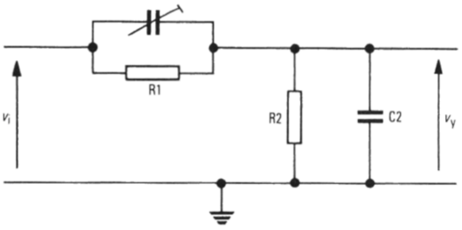


Figure 2

(*a*) *Show that under certain conditions the network is not frequency sensitive.*
(*b*) *Calculate the value of R1 when R2 is 1·2 MΩ, and given that C2 is 35 pF, find the correct setting for C1.*

A4 (*a*) By voltage division,

$$\frac{v_y}{v_i} = \frac{Z_2}{Z_1 + Z_2},$$

where Z_1 and Z_2 are the impedances of the series and shunt sections, respectively.

Using the 'product over sum' rule for the parallel sections,

$$Z_1 = \frac{R_1 \dfrac{1}{\mathrm{j}\omega C_1}}{R_1 + \dfrac{1}{\mathrm{j}\omega C_1}}.$$

$$= \frac{R_1}{1 + \mathrm{j}\omega C_1 R_1}.$$

Similarly,

$$Z_2 = \frac{R_2}{1 + \mathrm{j}\omega C_2 R_2}.$$

$$\therefore \qquad \frac{Z_2}{Z_1 + Z_2} = \frac{\dfrac{R_2}{1 + \mathrm{j}\omega C_2 R_2}}{\dfrac{R_1}{1 + \mathrm{j}\omega C_1 R_1} + \dfrac{R_2}{1 + \mathrm{j}\omega C_2 R_2}}.$$

Multiplying numerator and denominator by $1 + \mathrm{j}\omega C_2 R_2$,

$$\frac{Z_2}{Z_1 + Z_2} = \frac{R_2}{R_2 + R_1 \dfrac{(1 + \mathrm{j}\omega C_2 R_2)}{(1 + \mathrm{j}\omega C_1 R_1)}} = \frac{v_\mathrm{y}}{v_\mathrm{i}}.$$

When the variable capacitor is set such that $C_1 R_1 = C_2 R_2$,

$$\frac{v_\mathrm{y}}{v_\mathrm{i}} = \frac{R_2}{R_1 + R_2},$$

and the network becomes purely resistive.

(*b*) For an attenuation of 10 times,

$$\frac{v_\mathrm{y}}{v_\mathrm{i}} = \frac{1}{10} = \frac{R_2}{R_1 + R_2}.$$

$$\therefore \qquad 10R_2 = R_1 + R_2.$$

$$\therefore \qquad 9R_2 = R_1.$$

When

$$R_2 = 1{\cdot}2\ \mathrm{M\Omega},$$

$$R_1 = 9 \times 1{\cdot}2\ \mathrm{M\Omega}.$$

$$\therefore \qquad R_1 = 10{\cdot}8\ \mathrm{M\Omega}.$$

The correct setting for C_1 is when

$$C_1 R_1 = C_2 R_2.$$

$$\therefore \qquad C_1 = \frac{C_2 R_2}{R_1},$$

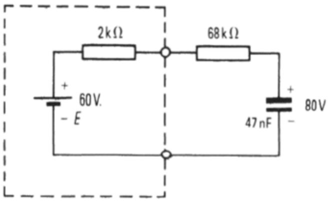
$$= \frac{35 \times 1{\cdot}2 \times 10^6}{10{\cdot}8 \times 10^6}\ \mathrm{pF}.$$

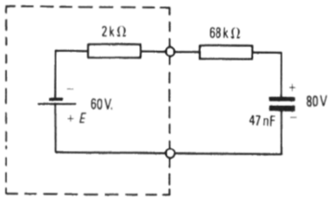
$$\therefore \qquad C_1 = \underline{3{\cdot}89\ \mathrm{pF}}.$$

Q5 *A 47 nF capacitor is charged via a 68 kΩ resistor until its potential difference reaches 80 V. The series combination is then disconnected from the charging source and connected to a power supply of EMF 60 V and internal resistance 2 kΩ.*

Calculate the potential difference across the capacitor 5 ms after the connection is made to the power supply for the two possible polarities of the supply.

A5





The potential difference after 5 ms can be found by combining the charging and discharging formulae for the capacitor.

The final potential difference is given by

$$V_c = V(1 - e^{-t/CR}) + V'e^{-t/CR},$$

where V assumes that, at $t = 0$, the capacitor is uncharged and charges from zero volts towards plus or minus 60 V.

V' assumes that the capacitor potential difference is 80 V at $t = 0$ and begins to discharge towards zero.

The method described is an interesting application of the superposition theorem.

The time constant in both cases is given by

$$\begin{aligned}\tau &= CR \text{ seconds,}\\ &= 47 \times 10^{-9} \times (68 + 2) \times 10^{3},\\ &= 3{\cdot}29 \times 10^{-3}\ \text{s.}\end{aligned}$$

After 5 ms,

$$\frac{t}{CR} = \frac{5 \times 10^{-3}}{3{\cdot}29 \times 10^{-3}} = 1{\cdot}5198.$$

When $E = +60$ V,

$$\begin{aligned}V_c &= 60(1 - e^{-1{\cdot}5198}) + 80e^{-1{\cdot}5198},\\ &= 60 - 60e^{-1{\cdot}5198} + 80e^{-1{\cdot}5198},\\ &= 60 + 20e^{-1{\cdot}5198},\\ &= \underline{64{\cdot}375\ \text{V.}}\end{aligned}$$

When $E = -60$ V,

$$\begin{aligned}V_c &= -60(1 - e^{-1{\cdot}5198}) + 80e^{-1{\cdot}5198},\\ &= -60 + 60e^{-1{\cdot}5198} + 80e^{-1{\cdot}5198},\\ &= -60 + 140e^{-1{\cdot}5198},\\ &= \underline{-29{\cdot}374\ \text{V.}}\end{aligned}$$

Q6 *The transistor shown in Figure 3 has a base current of 10 μA, which is determined by the bias network and the supply voltage of 10 V.*

When the base terminal of the transistor is disconnected, the potential difference across the 12 kΩ resistor is 2 V.

Calculate the value of the upper resistor R1, and find the base voltage when the transistor base terminal is connected.

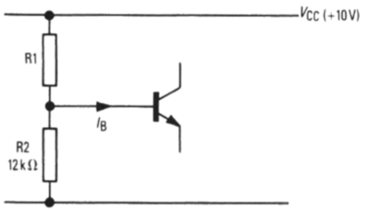


Figure 3

A6 By voltage division,

$$V_{R2} = V_{CC}\frac{R_2}{R_1 + R_2}.$$

$$\therefore \quad \frac{V_{R2}}{V_{CC}} = \frac{R_2}{R_1 + R_2}.$$

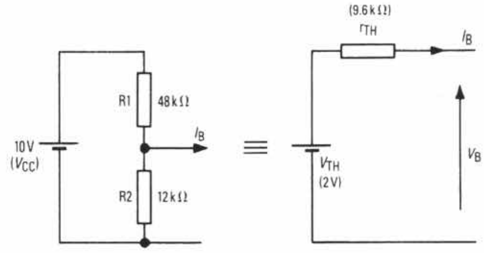
$$\therefore \quad R_1 + R_2 = R_2\frac{V_{CC}}{V_{R2}}.$$

$$\therefore \quad R_1 = \frac{R_2 V_{CC}}{V_{R2}} - R_2.$$

Substituting values,

$$R_1 = \left(\frac{12 \times 10}{2} - 12\right) \text{k}\Omega = \underline{48\ \text{k}\Omega.}$$

To find the base voltage when base current flows, a Thèvenin equivalent circuit can be drawn. When the base is disconnected, the circuit is as shown in the sketch.



As given in the question, the open circuit voltage (V_{TH}) is 2 V.
r_{TH} is the value of R_1 and R_2 in parallel.

$$\therefore \quad \frac{1}{r_{TH}} = \left(\frac{1}{12} + \frac{1}{48}\right) \times 10^{-3}.$$

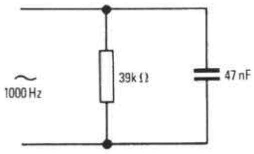
$$\therefore \quad r_{TH} = 9{\cdot}6\ \text{k}\Omega.$$

When base current flows,

$$\begin{aligned} V_B &= V_{TH} - V_{r_{TH}}, \\ &= V_{TH} - I_B r_{TH}, \\ &= 2 - (10 \times 10^{-6} \times 9{\cdot}6 \times 10^3), \\ &= \underline{1{\cdot}904\ \text{V.}} \end{aligned}$$

Q7 A resistor of 39 kΩ is placed in parallel with a capacitor of 47 nF. Calculate the admittance, conductance and susceptance of the circuit when the applied frequency is 1000 Hz.

A7 The sketch shows the circuit.



For the parallel circuit

$$\frac{1}{Z} = Y = \frac{1}{R} + \frac{1}{\dfrac{1}{j\omega C}},$$

$$\therefore \quad Y = \frac{1}{R} + j\omega C.$$

This is of the form $Y = G + jB$.

$$\omega C = 2\pi 1000 \times 47 \times 10^{-9},$$

$$= 295{\cdot}3 \times 10^{-6}\ \text{S}.$$

$$\therefore \quad Y = \frac{1}{39\,000} + j295{\cdot}3 \times 10^{-6}\ \text{S},$$

$$= (25{\cdot}64 + j295{\cdot}3)10^{-6}\ \text{S}.$$

$$|Y| = \sqrt{(25{\cdot}64^2 + 295{\cdot}3^2)} \times 10^{-6} = 296{\cdot}4 \times 10^{-6}\ \text{S}.$$

By comparison with the general form,

$$Y = \underline{296{\cdot}4\ \mu\text{S}.}$$

$$G = \underline{25{\cdot}64\ \mu\text{S}.}$$

$$B = \underline{295{\cdot}3\ \mu\text{S}.}$$

Q8 *On analysis, the output signal of an amplifier is found to contain 20 V at the fundamental frequency of the applied test signal, 5 V at its second harmonic and 1·4 V at its third harmonic.*

(*a*) *Calculate the power dissipated in a load of 600 Ω.*
(*b*) *What percentage harmonic distortion is present*

(*i*) *in the output voltage, and*
(*ii*) *in the output power?*

A8 (*a*) The RMS voltage of a complex wave is given by

$$V = \sqrt{(V_F^2 + V_{2H}^2 + V_{3H}^2 + \ldots)},$$

where V_F is the RMS value of the fundamental,
V_{2H} is the RMS value of the second harmonic, etc.

$$\therefore \quad V = \sqrt{(20^2 + 5^2 + 1{\cdot}4^2)} = 20{\cdot}663\ \text{V}.$$

The power dissipated in the load is given by:

$$P = \frac{V^2}{R_L} = \frac{20{\cdot}663^2}{600}\ \text{W} = \underline{0{\cdot}71\ \text{W}.}$$

(*b*) (*i*) The percentage harmonic distortion is given by

$$\frac{\sqrt{(V_{2H}^2 + V_{3H}^2 + \ldots)}}{V_F} \times 100\%$$

Therefore, harmonic distortion in the output voltage

$$= \frac{\sqrt{(5^2 + 1{\cdot}4^2)}}{20} \times 100\% = \frac{5{\cdot}19}{20} \times 100\% = \underline{25{\cdot}96\%.}$$

(*ii*) The power is proportional to the square of the voltage. Therefore, the harmonic distortion in the output power

$$= \left(\frac{5{\cdot}19}{20}\right)^2 \times 100\% = \underline{6{\cdot}734\%.}$$

Q9 *An alternator produces an RMS voltage of 250 V at 50 Hz, but the output waveform contains 10% second harmonic and 6% third harmonic components.*

Calculate the RMS value of the three components of the voltage, and write down the expression for the alternator output. Assume that all components are sine waves.

A9

$$V_{\mathrm{RMS}} = \sqrt{(V_{\mathrm{F}}^2 + V_{\mathrm{2H}}^2 + V_{\mathrm{3H}}^2)}.$$

Since the second harmonic represents 10% of the value of the fundamental,

$$V_{\mathrm{2H}} = 0{\cdot}1\,V_{\mathrm{F}}.$$

Similarly, $$V_{\mathrm{3H}} = 0{\cdot}06\,V_{\mathrm{F}}.$$

$$\begin{aligned}
\therefore \quad V_{\mathrm{RMS}} &= \sqrt{\{V_{\mathrm{F}}^2 + (0{\cdot}1\,V_{\mathrm{F}})^2 + (0{\cdot}06\,V_{\mathrm{F}})^2\}}, \\
&= V_{\mathrm{F}}\sqrt{(1 + 0{\cdot}1^2 + 0{\cdot}06^2)}, \\
&= V_{\mathrm{F}}\sqrt{1{\cdot}0136}.
\end{aligned}$$

$$\begin{aligned}
\therefore \quad V_{\mathrm{F}} &= \frac{V_{\mathrm{RMS}}}{\sqrt{1{\cdot}0136}}, \\
&= \frac{250}{\sqrt{1{\cdot}0136}} = \underline{248{\cdot}3\ \mathrm{V}.}
\end{aligned}$$

From which,

$$V_{\mathrm{2H}} = 0{\cdot}1 \times 248{\cdot}3 = \underline{24{\cdot}83\ \mathrm{V},}\ \text{and}$$

$$V_{\mathrm{3H}} = 0{\cdot}06 \times 248{\cdot}3 = \underline{14{\cdot}898\ \mathrm{V}.}$$

The expression for the alternator output as given by

$$v = V_{\mathrm{F}} \sin \omega t + V_{\mathrm{2H}} \sin 2\omega t + V_{\mathrm{3H}} \sin 3\omega t \text{ volts},$$

where V is the peak voltage and ω is the fundamental angular frequency.

$$\omega = 2\pi f = 2\pi \times 50 = 100\pi \text{ rad/s}.$$

$$\begin{aligned}
\therefore \quad v &= 284{\cdot}3\sqrt{2} \sin 100\pi t + 24{\cdot}83\sqrt{2} \sin 200\pi t + 14{\cdot}898\sqrt{2} \sin 300\pi t \text{ volts}. \\
&= \underline{351 \sin 100\pi t + 35{\cdot}1 \sin 200\pi t + 21 \sin 300\pi t \text{ volts}.}
\end{aligned}$$

PART 2—Electronics (Digital) IV (BTEC)

Q10 *(a) Draw the Karnaugh maps for the direct and inverse functions of*

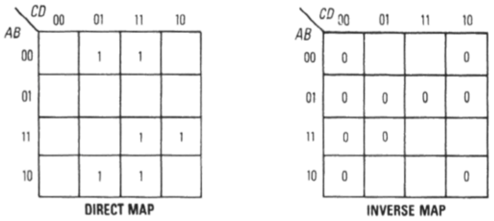
$$F(A\,B\,C\,D) = \Sigma\, 1, 3, 9, 11, 14, 15.$$

(b) Using the inverse map, obtain the minimal expression for the function.
(c) From the minimal expression of part (b) obtain an expression using only NOR *gates and draw the logic diagram.*

A10

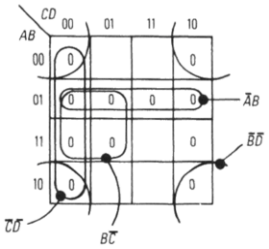
> The Sigma notation gives a shorthand method of writing down the function and obviates the need to take extra care about the placing of any negation bars over the appropriate letters. The symbol $F(A\,B\,C\,D)$ indicates that there are four variables and that A is the most significant bit. The maps should be drawn with AB vertical and CD horizontal so that the binary value can be read off directly; for example. $3 \equiv 0011_2 \equiv \bar{A}\bar{B}CD$.

(*a*)



DIRECT MAP INVERSE MAP

(*b*)



Note that $\bar{B}\bar{D}$ represents a group of four terms obtained because on the Karnaugh map the corners are next to each other.

The function obtained for the inverse map is $\bar{F}$.

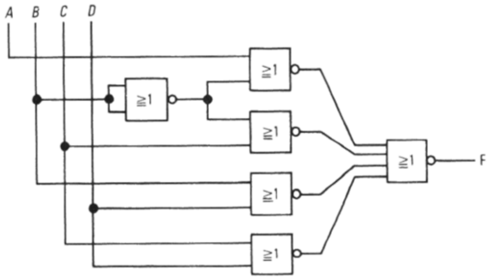
$$\therefore \qquad \bar{F} = \bar{A}B + B\bar{C} + \bar{B}\bar{D} + \bar{C}\bar{D}.$$

$$\therefore \qquad F = \overline{\bar{A}B + B\bar{C} + \bar{B}\bar{D} + \bar{C}\bar{D}}.$$

(*c*) This expression provides a NOR gate at the output, but the individual groups are in AND form. These can be converted by the use of De Morgan's law.

$$\therefore \qquad F = \overline{\overline{(A+\bar{B})} + \overline{(\bar{B}+C)} + \overline{(B+D)} + \overline{(C+D)}}.$$

See sketch.



Q11 (*a*) *Draw the Karnaugh map for the function*

$$F(W\,X\,Y\,Z) = \Sigma 0,\ 1,\ 2,\ 4,\ 6,\ 8,\ 9,\ 14,\ 15,$$

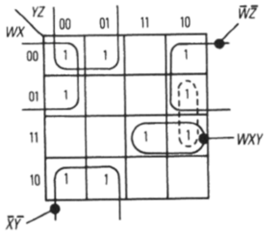
and obtain the minimal expression.

(*b*) *By inspection of the map, determine whether a static hazard will be produced by the minimal function and if so explain why.*

(*c*) *Modify the expression in part* (*a*) *to avoid the presence of a static hazard if one exists.*

(*d*) *Draw the static hazard-free logic circuit using only* NAND *gates.*

A11 (*a*)



$$F = \bar{X}\bar{Y} + \bar{W}\bar{Z} + WXY.$$

(*b*) Reference to the map shows that the term WXY is not linked with the other terms and therefore a static '1' hazard occurs.

The static '1' hazard occurs when the variable W changes from '1' to '0'. The hazard occurs because of the transmission delay which causes $\bar{W}$ to change slightly later at the output of the inverter than W at the input to the inverter.

(*c*) The static hazard can be removed by adding a term which links WXY with the other terms in the minimal function. This is shown dotted on the map.

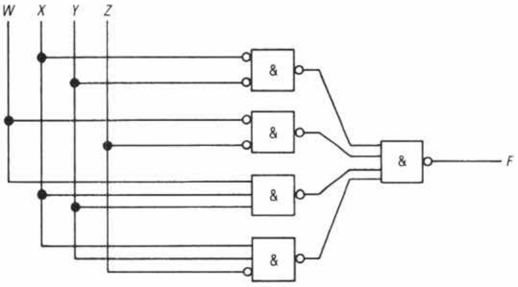
$$\text{Added term} = XY\bar{Z}.$$

The static hazard-free function now becomes

$$F = \bar{X}\bar{Y} + \bar{W}\bar{Z} + WXY + XY\bar{Z}.$$

(*d*) Using de Morgan's law to convert to NAND logic,

$$F = \overline{\overline{(\bar{X}\bar{Y})}\,\overline{(\bar{W}\bar{Z})}\,\overline{(WXY)}\,\overline{(XY\bar{Z})}}.$$



Q12 A four-stage feedback shift register has modulo-two feedback from stages P and R, where P is the most significant bit and the stages are P, Q, R and S. Given that the register initially contains 0010_2:

(a) Draw up a table showing the external states and the feedback signal and obtain the random sequence.

(b) Find the cycle length.

(c) Write down the state sequence.

(d) Is the cycle length the maximum possible for this number of stages in a feedback shift register?

A12 (*a*)

STATE	P	Q	R	S	P ⊕ R
S_2	0	0	1	0	1
S_5	0	1	0	1	0
S_{10}	1	0	1	0	0
S_4	0	1	0	0	0
S_8	1	0	0	0	1
S_1	0	0	0	1	0
S_2	0	0	1	0	

(*b*) By inspection, the cycle repeats after S_1, so the cycle length is 6.

(*c*) The state sequence is given by

$$S_2 \rightarrow S_5 \rightarrow S_{10} \rightarrow S_4 \rightarrow S_8 \rightarrow S_1 \rightarrow S_2$$

(*d*) The maximum length sequence (MLS) is given by

$$\text{MLS} = 2^n - 1,$$

where n is the number of stages.

So that for four stages

$$\text{MLS} = 2^4 - 1 = 15.$$

> Note that S_0 is not produced because, if the sequence enters 0000_2, there are no signals to generate feedback from the 'modulo two' circuit. The MLS for a four-stage feedback register occurs when feedback is from the two most significant stages; that is, $F = P \oplus Q$.

Q13 Figure 4 shows the output transistor of a TTL gate. The base drive current is 25 μA and $h_{FE} = 28$. Determine whether the circuit satisfies the requirements of TTL operation.

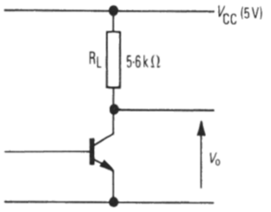


Figure 4

A13 When the base current is applied, the collector voltage falls in order to output a '0'. The collector voltage is given by

$$V_C = V_{CC} - V_{R_L} = V_{CC} - I_C R_L, \text{ where } I_C = h_{FE} I_B.$$

$$\therefore \quad I_C = 28 \times 25 \times 10^{-6}\,\text{A} = 0{\cdot}7\,\text{mA}.$$

$$V_0 = V_C = 5 - 0{\cdot}7 \times 10^{-3} \times 5600 = 1{\cdot}08\,\text{V}.$$

For the requirements of TTL to be satisfied, the voltage levels must be as follows:

2 V–5 V	'1'
0 V–0·8 V	'0'

Since V_0 is above 0·8 V the circuit requirements do not satisfy TTL working.

In order that V_0 falls at least to 0·8 V, the base current must be increased. The minimum value of I_C is given by $\dfrac{V_{CC} - V_C}{R_L}$.

$$I_C = \frac{5 - 0{\cdot}8}{5600} = 0{\cdot}75\,\text{mA},$$

and the minimum value of I_B is $\dfrac{I_C}{h_{FE}}$.

$$\therefore \quad I_B = \frac{0{\cdot}75 \times 10^{-3}}{28} = 26{\cdot}786\,\mu\text{A}.$$

Note that, when a load is connected to the output of the gate, voltage division takes place between R_L and the external load. Care must be taken that V_0 is at least 2 V when the base current is removed and the transistor reverts to its non-conducting condition.

Q14 (*a*) *For the logic diagram shown in Figure 5, obtain the output function.*
(*b*) *Using Boolean algebra, show that the output represents the sum of two binary digits.*
(*c*) *Explain where the circuit finds application.*

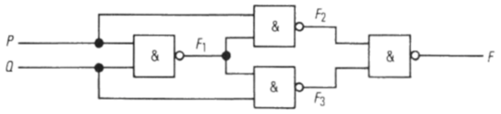


Figure 5

A14 (*a*)

$$F_1 = \overline{PQ}.$$

$$F_2 = \overline{PF_1} = \overline{P(\overline{PQ})}.$$

$$F_3 = \overline{QF_1} = \overline{Q(\overline{PQ})}.$$

$$F = \overline{F_2 F_3}.$$

$$\therefore \quad F = \overline{(\overline{P(\overline{PQ})})(\overline{Q(\overline{PQ})})}.$$

(*b*) By de Morgan's theorem,

$$\overline{PQ}=\bar{P}+\bar{Q}.$$

$$\therefore \quad F=\overline{\overline{P(\bar{P}+\bar{Q})}\;\overline{Q(\bar{P}+\bar{Q})}},$$

$$=\overline{\overline{(P\bar{P}+P\bar{Q})}\;\overline{(Q\bar{P}+Q\bar{Q})}}.$$

But $P\bar{P}=0$ and $Q\bar{Q}=0$.

$$\therefore \quad F=\overline{\overline{(P\bar{Q})}\;\overline{(Q\bar{P})}}$$

Again, using de Morgan's theorem,

$$F=P\bar{Q}+Q\bar{P}=P\oplus Q.$$

This expression is the EXCLUSIVE-OR function.

Drawing the truth table for the addition of two binary digits shows that the function will produce the sum of those two digits.

P	Q	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0 →	1

(*c*) The logic circuit can be employed as part of the half-adder circuit used for binary addition.

The logic circuit also finds application where disparity between two bits must be identified; that is, when the two bits are different, the output is a '1'.

Q15 *Figure 6 shows the circuit of a discrete-component TTL tri-state inverting buffer similar to that used in digital systems.*

(*a*) *Explain the term 'tri-state'.*
(*b*) *Draw the truth table for the circuit shown.*
(*c*) *Explain the operation of the circuit under tri-state conditions.*

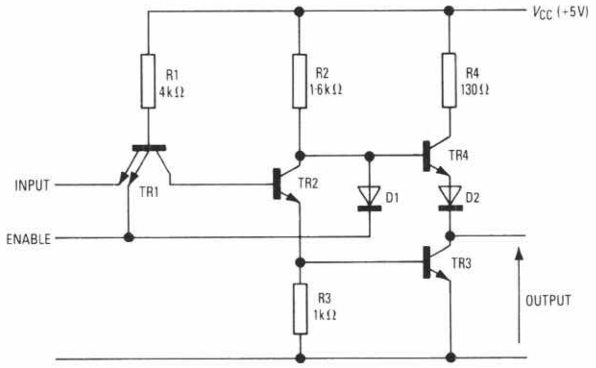


Figure 6

A15 (*a*) The term *tri-state* refers to a digital circuit in which the output can be in one of three states. When in the tri-state condition, the impedance seen 'looking in' at the output terminal is very high and effectively open circuit. When not in the tri-state condition, the output is either '1' or '0'.

(*b*)

INPUT	ENABLE	OUTPUT
0	0	HIGH Z
0	1	1
1	0	HIGH Z
1	1	0

(*c*) From the truth table it is seen that, when ENABLE = 0, the device is in the tri-state. Current flows through resistor R1 and the base–emitter junction of transistor TR1 so that the base voltage goes to $V_{\mathrm{BE,SAT}}=0{\cdot}8$ V. When this occurs, the potential difference across the base–collector junction of TR1 in series with the base–emitter junctions of TR2 and TR3 is insufficient to bring TR2 and TR3 into conduction (a potential difference of at least 1·65 V would be required since $V_{\mathrm{BE,ON}}\approx 0{\cdot}55$ V). Thus transistor TR3 is non-conducting and in the high-impedance state.

Current also flows through resistor R2 and diode D1 so that the anode of D1 is held at some 0·75 V. Again, the potential difference across the base–emitter junction of TR4 and D2 is insufficient to bring TR4 into conduction, so that TR4 is also in the high-impedance state.

Since both TR3 and TR4 are non-conducting, except for any leakage resistance, the output terminal is isolated from the circuit; that is, high impedance.

Q16 *For the tri-state buffer of Figure 6, calculate the power consumption of the complete circuit when in the tri-state condition. Assume that the transistor leakage current (I_{CEO}) is zero and that the* ENABLE *line is at zero volts.*

A16

> Under the tri-state condition transistors TR2, TR3 and TR4 are non-conducting (see problem Q15). Current flows through the enabling emitter and through diode D1. This means that the total current taken from the supply is via resistors R1 and R2.

Taking $V_{\mathrm{BE,SAT}} = 0{\cdot}8$ V and $V_{\mathrm{AK}} = 0{\cdot}8$ V,

$$I_{\mathrm{R1}} = \frac{V_{\mathrm{cc}} - V_{\mathrm{BE,SAT}}}{R_1}.$$

Substituting values,

$$I_{\mathrm{R1}} = \frac{5 - 0{\cdot}8}{4000}\ \mathrm{A},$$

$$= 1{\cdot}05\ \mathrm{mA}.$$

$$I_{\mathrm{R2}} = \frac{V_{\mathrm{cc}} - V_{\mathrm{AK(D1)}}}{R_2},$$

$$= \frac{5 - 0{\cdot}8}{1600}\ \mathrm{A},$$

$$= 2{\cdot}625\ \mathrm{mA}.$$

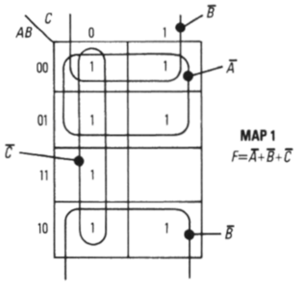
$$I_{\mathrm{T}} = I_{\mathrm{R1}} + I_{\mathrm{R2}} = (1{\cdot}05 + 2{\cdot}625)\ \mathrm{mA} = 3{\cdot}675\ \mathrm{mA},$$

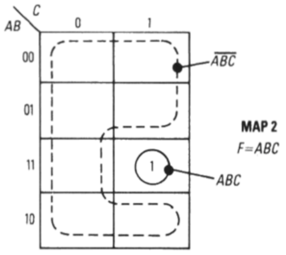
$$\text{Power} = I_{\mathrm{T}} V_{\mathrm{cc}} = 3{\cdot}675 \times 10^{-3} \times 5 = \underline{18{\cdot}375\ \mathrm{mW}.}$$

Q17 *Show by Karnaugh mapping that*

$$\overline{ABC} \equiv \bar{A} + \bar{B} + \bar{C}.$$

A17





By inspection it can be seen that the unoccupied squares on Map 2 represent the *INVERSE* map. Thus, if the only occupied square is *ABC*, then the rest of the map is $\overline{ABC}$ or that given by $\bar{A} + \bar{B} + \bar{C}$ on Map 1.

> The equivalence sign is given in the question because the two logic equations require differing circuit arrangements. $\overline{ABC}$ requires a single NAND gate, whereas $\bar{A} + \bar{B} + \bar{C}$ requires an OR gate preceded by three inverters. From a practical point of view, the transmission time through the two equivalent circuits may be different.

Part 3—Electronics IV (BTEC)

Q18 *Figure 7 shows the circuit of a transistor amplifier with a tuned load, connected in common-emitter mode. The transistor parameters are*

$$h_{fe} = 54,\ h_{oe} = 25\ \mu S \text{ and } h_{ie} = 1250\ \Omega,$$

and the inductor has an effective resistance of 89·53 Ω at the frequency of resonance.

(a) Calculate the frequency of resonance and the dynamic impedance for the tuned circuit. Thus find the tuned circuit bandwidth.

(b) Draw the equivalent circuit for the circuit of Figure 7.

(c) Find the voltage gain for the circuit at the frequency of resonance.

(d) Calculate the Q of the complete circuit and show that the circuit bandwidth is greater than that for the LC circuit taken separately.

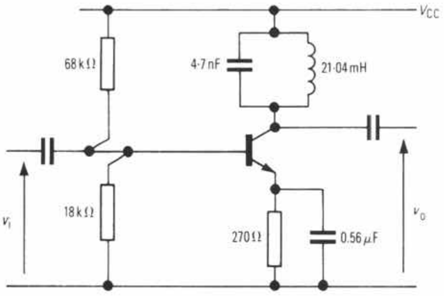


Figure 7

A18 (*a*) To a very good approximation the formula $f = \frac{1}{2\pi\sqrt{(LC)}}$ may be used to calculate the frequency of resonance.

$$\therefore \quad f = \frac{1}{2\pi\sqrt{(21{\cdot}04 \times 10^{-3} \times 4{\cdot}7 \times 10^{-9})}}\ \text{Hz} = \underline{16\ \text{kHz.}}$$

The dynamic impedance is given by

$$Z_D = \frac{L}{Cr} = \frac{21{\cdot}04 \times 10^{-3}}{4{\cdot}7 \times 10^{-9} \times 89{\cdot}53}\ \Omega = \underline{50\ \text{k}\Omega.}$$

The bandwidth can be obtained by using the relationship

$$\text{bandwidth} = \frac{f_R}{Q}.$$

But firstly the Q must be obtained. Care is needed here because Q for a parallel circuit is given by $\frac{R}{X}$. In this case, R is the dynamic impedance Z_D.

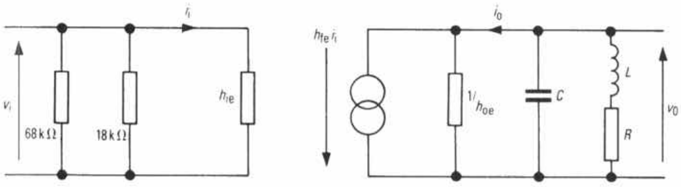
$$Q = \frac{Z_D}{1/(\omega_0 C)} = Z_D \omega_0 C$$

where ω_0 is the angular resonance frequency.

$$\therefore \quad Q = 50 \times 10^3 \times 2\pi \times 16 \times 10^3 \times 4{\cdot}7 \times 10^{-9} = 23{\cdot}625.$$

$$\text{Thus, bandwidth} = \frac{f_R}{Q} = \frac{16\,000}{23{\cdot}625}\ \text{Hz} = \underline{677\ \text{Hz.}}$$

(*b*)



The emitter resistor is not shown because it is effectively decoupled by the emitter decoupling capacitor.

(*c*) At the frequency of resonance, the tuned circuit behaves as a pure resistance of Z_D ohms and this is in parallel with $1/h_{oe}$. These two together form the load for the transistor (Z_L).

$$\frac{1}{Z_L} = \frac{1}{Z_D} + h_{oe},$$

$$= \frac{1}{50\,000} + (25 \times 10^{-6}).$$

$$\therefore \quad Z_L = 22{\cdot}22\ \mathrm{k\Omega}.$$

The voltage gain is given by

$$A_v = -\frac{h_{fe}Z_L}{h_{ie}},$$

$$= -\frac{54 \times 22{\cdot}22 \times 10^3}{1250},$$

$$= \underline{-959{\cdot}9.}$$

(*d*) The effect of connecting the tuned circuit to the transistor is to place $1/h_{oe}$ across Z_D and thus reduce the dynamic impedance and lower the Q. The new value of Q is found as in (*a*), but by using Z_L instead of Z_D.

$$\therefore \quad Q = Z_L\omega_0 C,$$

$$= 22{\cdot}22 \times 10^3 \times 2\pi \times 16 \times 10^3 \times 4{\cdot}7 \times 10^{-9},$$

$$= 10{\cdot}5.$$

$$\text{The modified bandwidth} = \frac{f_R}{Q} = \frac{16\,000}{10{\cdot}5}\ \mathrm{Hz} = \underline{1523{\cdot}8\ \mathrm{Hz}.}$$

> It should be noted that, if the circuit were used to drive a successive stage, the loading effect of that stage would again cause the voltage gain to be reduced and the bandwidth to be modified. Strictly speaking, h_{oe} is an admittance made up of both resistance and capacitance but the capacitance is only a few picofarads. This, in practice, causes the frequency of resonance to be slightly lower, but since the percentage change when compared with the value of 4·7 nF is small, it is justifiable to treat h_{oe} as if it were purely resistive.

Q19 *Figure 8 shows an operational amplifier connected as an inverting summing amplifier. The input signal to resistor R1 is −0·5 V and that to R2 is a 2 V, 1000 Hz sine wave.*

Obtain the equation for the output voltage and sketch the output waveform, showing both voltage levels and time intervals.

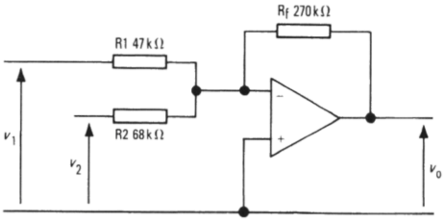


Figure 8

A19 For the inverting summing amplifier, the output voltage is given by

$$v_0 = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2\right),$$

but firstly the equation for the sine wave must be obtained.

$$v = V \sin \omega t,$$

where $V = 2\sqrt{2}$ volts, and $\omega = 2\pi f = 2\pi 1000 = 2000\pi$ rad/s.

$$\therefore \qquad v_2 = 2\sqrt{2} \sin 2000\pi t \text{ volts.}$$

Substituting the values of v_1 and v_2,

$$v_o = -\left\{\frac{270}{47}(-0{\cdot}5) + \frac{270}{68}(2\sqrt{2} \sin 2000\pi t)\right\} \text{ volts,}$$

$$= \underline{2{\cdot}872 - 11{\cdot}23 \sin 2000\pi t \text{ volts.}}$$

The output voltage equation shows that the output consists of a minus sine wave superimposed on a positive DC level.

The range of output voltage is between

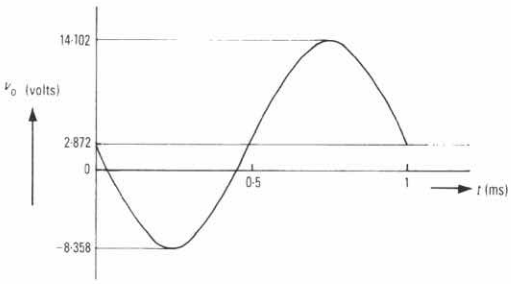
$$2{\cdot}872 - 11{\cdot}23 = -8{\cdot}358 \text{ V, and}$$

$$2{\cdot}872 + 11{\cdot}23 = +14{\cdot}102 \text{ V,}$$

and the periodic time is

$$T = \frac{1}{f} = \frac{1}{1000} \text{ s} = 1 \text{ ms.}$$

The waveform is shown in the sketch.



> This circuit finds application where it is desired to obtain an AC waveform superimposed on a DC level. By making v_1 a variable DC supply, it is possible to shift the DC level of the output signal such that it can be either positive or negative or removed completely to give a pure AC waveform. This would be useful in a signal generator which is used to test equipment with differing specifications.

Q20 *Figure 9 shows the circuit of an operational amplifier connected as a sine wave oscillator. The output is taken directly from the output of the amplifier and the feedback is taken from the junction of the series and parallel networks.*

(*a*) *Give the name of the oscillator.*

(*b*) *Calculate the frequency of oscillation.*

(*c*) *Find the attenuation which occurs in the series, parallel network at the frequency of oscillation.*

(*d*) *Draw a sketch to show what modifications must be made to the circuit in order that the output shall be a pure sine wave. Also suggest values for any components which are introduced.*

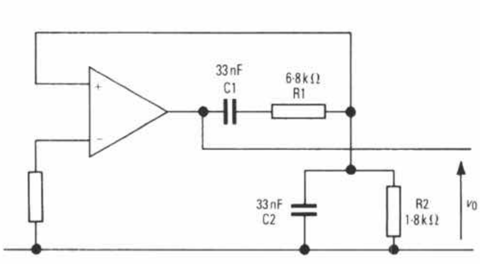


Figure 9

A20 (*a*) The circuit shown is a Wien bridge oscillator.

(*b*) The frequency of oscillation is determined by the Wien network and is given by

$$f = \frac{1}{2\pi\sqrt{(C_1 C_2 R_1 R_2)}} \text{ Hz.}$$

Since $C_1 = C_2 = C$,

$$\begin{aligned} f &= \frac{1}{2\pi C\sqrt{(R_1 R_2)}}, \\ &= \frac{1}{2\pi \times 33 \times 10^{-9}\sqrt{(6{\cdot}8 \times 10^3 \times 1{\cdot}8 \times 10^3)}}, \\ &= \underline{1378{\cdot}5\ \text{Hz.}} \end{aligned}$$

(*c*) At the frequency of oscillation, the network attenuation is given by

$$n = \frac{C_1 R_1 + C_2 R_2 + C_1 R_2}{C_1 R_2}.$$

When $C_1 = C_2 = C$ and $R_1 = R_2 = R$, the attenuation is a factor of three times, but in this case it is not so although $C_1 = C_2 = C$. The formula for attenuation can be tidied up as follows:

$$\begin{aligned} n &= \frac{CR_1 + CR_2 + CR_2}{CR_2}, \\ &= \frac{R_1 + R_2 + R_2}{R_2}, \\ &= \frac{R_1}{R_2} + 2 \qquad \text{(when } C_1 = C_2 = C\text{).} \end{aligned}$$

Substituting values,

$$n = \frac{6{\cdot}8}{1{\cdot}8} + 2 = \underline{5{\cdot}78.}$$

(*d*)

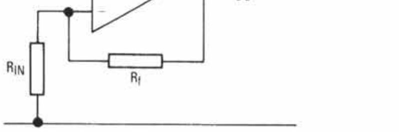
Typically, the intrinsic voltage gain of an operational amplifier is some 90 dB. This, as a voltage ratio, is

$$v_0 : v_i = 10^{90/20} = 31\,622{\cdot}8.$$

For sine wave oscillation, the loop gain must be unity and, therefore, βA_v must be unity. Negative feedback must be applied so that the amplifier voltage gain is reduced to 5·78. If this is not done, the operational amplifier rapidly goes into saturation. If this occurs, the circuit becomes a relaxation oscillator and the frequency of oscillation is no longer related to the previously given formula.

Negative feedback is applied by adding a feedback resistor, from the operational amplifier output to the inverting input terminal.

The modification to the circuit is shown in the sketch.



Suggesting a value of $R_f = 220\,\text{k}\Omega$ and using the relationship $A'_v = 1 + \frac{R_f}{R_{IN}}$ for the non-inverting amplifier,

$$R_{IN} = \frac{R_f}{A'_v - 1} = \frac{220 \times 10^3}{5{\cdot}78 - 1}\,\Omega = 46\,\text{k}\Omega.$$

> A practical value of 47 kΩ can be used for R_{1N}. In order to obtain good sinusoidal oscillation with no distortion, resistor R1 can be made a variable resistor, which can be adjusted to give the best output waveform. In signal generators, where long-term stability is required, it is usual to incorporate thermistor beads in the feedback circuits to compensate for variations in the circuit which result in either cessation of oscillation or distortion.

Q21 *The circuit shown in Figure 10 is an audio frequency amplifier using an FET. The FET has a mutual conductance of 4·3 mS and a gate-to-source input resistance of 365 kΩ.*

(a) Calculate the midband voltage gain of the circuit.

(b) By using the value obtained in part (a), calculate the midband voltage gain and circuit input resistance when the source decoupling capacitor is removed.

(c) What is the lowest frequency at which the 47 μF capacitor effectively decouples the source resistor?

(d) If the lowest input frequency is 150 Hz, what preferred value of capacitor should be used for C1?

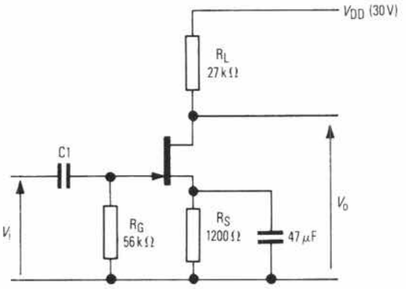


Figure 10

A21 (*a*) For the circuit given,

$$A_v = -g_m \frac{r_{DS} R_L}{r_{DS} + R_L},$$

where r_{DS} is the drain source resistance.

> When r_{DS} is not given, it may be assumed that its value is very high compared with R_L, and then

$$\begin{aligned} A_v &= -g_m R_L, \\ &= -4{\cdot}3 \times 10^{-3} \times 27 \times 10^3, \\ &= \underline{-116{\cdot}1.} \end{aligned}$$

(*b*) When the decoupling capacitor is removed, negative feedback is applied and the voltage gain is reduced to

$$A'_v = -\frac{A_v}{1 + \beta A_v},$$

where, when $R_L \gg R_s$, $\beta = \frac{R_s}{R_L}$.

$$\beta = \frac{1200}{27\,000} = \frac{1}{22{\cdot}5}.$$

$$\therefore \quad A'_v = -\frac{116{\cdot}1}{1+\left(\dfrac{1}{22{\cdot}5}\times 116{\cdot}1\right)},$$

$$= -18{\cdot}85.$$

When the decoupling capacitor is removed, series negative feedback is applied to the circuit and the input impedance of the transistor rises from Z_i to

$$Z'_i = Z_i(1+\beta A_v), \qquad \text{where } Z_i = r_{GS}.$$

$$\therefore \quad Z'_i = r_{GS}(1+\beta A_v),$$

$$= 365\left\{1+\left(\frac{1}{22{\cdot}5}\times 116{\cdot}1\right)\right\}\ \text{k}\Omega,$$

$$= 2{\cdot}248\ \text{M}\Omega.$$

The midband input resistance of the circuit is given by R_G in parallel with Z'_i.

$$\therefore \quad Z'_{i(\text{CIRCUIT})} = R_G//Z'_i = 56//2248\ \text{k}\Omega = \underline{54{\cdot}64\ \text{k}\Omega.}$$

(*c*) Using the rule of thumb that the capacitive reactance should be one tenth of the value of the resistor being decoupled at the lowest frequency.

$$X_C = \frac{1}{10}R_s.$$

$$\therefore \quad \frac{1}{2\pi f C_s} = \frac{R_s}{10}.$$

$$\therefore \quad f = \frac{1}{2\pi C_s \dfrac{R_s}{10}}\ \text{Hz},$$

$$= \frac{1}{2\pi\times 47\times 10^{-6}\times 120}\ \text{Hz},$$

$$= \underline{28{\cdot}2\ \text{Hz.}}$$

(*d*) The same rule of thumb is used here, where

$$X_{C1} = \frac{Z_{i(\text{CIRCUIT})}}{10}.$$

$Z_{i(\text{CIRCUIT})}$ (when R_s decoupled) $= R_G//r_{GS}$.

$$R_G//r_{GS} = 56//365\ \text{k}\Omega = 48{\cdot}55\ \text{k}\Omega.$$

$$\therefore \quad X_C = 4{\cdot}855\ \text{k}\Omega.$$

$$\frac{1}{2\pi f C} = 4{\cdot}855\times 10^3.$$

$$\therefore \quad C = \frac{1}{2\pi f\times 4{\cdot}855\times 10^3}.$$

At the lowest input frequency of 150 Hz,

$$C = \frac{1}{2\pi\times 150\times 4{\cdot}855\times 10^3}\ \text{F},$$

$$= 0{\cdot}219\ \mu\text{F}.$$

Using the nearest larger preferred value of capacitor, a capacitor not smaller than $\underline{0{\cdot}22\ \mu\text{F}}$ should be used.

Q22 *(a) An amplifier with an intrinsic voltage gain of 1800 has 2% negative feedback applied. Calculate the overall voltage gain with negative feedback.*

(b) A second amplifier has an intrinsic voltage gain of 80. Find the amount of negative feedback which must be applied to give the same overall voltage gain as the amplifier in part (a).

(c) Over a period of one year, both amplifiers deteriorate such that their intrinsic voltage gain falls by 15%. Calculate, for both amplifiers, the percentage change in overall voltage gain after this period when negative feedback is applied.

(d) Comment on the relative merits of both arrangements.

A22 (*a*) Using the negative feedback equation

$$A'_v = \frac{A_v}{1+\beta A_v},$$

$$= \frac{1800}{1+\left(\frac{2}{100}\times 1800\right)},$$

$$= \underline{48{\cdot}649.}$$

(*b*) Transposing the negative feedback equation for β,

$$A'_v = \frac{A_v}{1+\beta A_v}.$$

$$\therefore \quad 1+\beta A_v = \frac{A_v}{A'_v}.$$

$$\therefore \quad \beta A_v = \frac{A_v}{A'_v} - 1.$$

$$\therefore \quad \beta = \left(\frac{A_v}{A'_v} - 1\right)\frac{1}{A_v},$$

$$= \left(\frac{80}{48{\cdot}649} - 1\right)\frac{1}{80},$$

$$= 0{\cdot}0081 = \underline{0{\cdot}81\%.}$$

(*c*) After one year, A_v will fall to $A_{v,1} = A_v\left(\frac{100-15}{100}\right)$. For the two amplifiers, A and B,

$$A_{v,A,1} = \frac{1800\times 85}{100} = 1530, \text{ and}$$

$$A_{v,B,1} = \frac{80\times 85}{100} = 68.$$

Substituting these values into the negative feedback equation,

$$A'_{v,A,1} = \frac{1530}{1+\left(\frac{2}{100}\times 1530\right)} = 48{\cdot}4.$$

$$A'_{v,B,1} = \frac{68}{1+\left(\frac{0{\cdot}81}{100}\times 68\right)} = 43{\cdot}85.$$

Percentage change for amplifier A.

$$= \frac{48{\cdot}649 - 48{\cdot}4}{48{\cdot}649}\times 100\% = \underline{0{\cdot}51\%.}$$

Percentage change for amplifier B

$$= \frac{48{\cdot}649 - 43{\cdot}85}{48{\cdot}649} \times 100\% = \underline{9{\cdot}86\%.}$$

(*d*) The deterioration in overall voltage gain with negative feedback after the period of one year is some 19 times worse when the amplifier of low intrinsic voltage gain is used. This suggests that, when an overall voltage gain of a given value is required, it is better to use a high intrinsic gain with much feedback than an amplifier with low intrinsic gain and little feedback. In the extreme case, an amplifier of intrinsic gain 48·649 would require no negative feedback, but would deteriorate by 15% in the same period.

> Care must be taken, however. If the intrinsic-high-gain amplifier is multi-stage, the coupling components may produce some phase shift. At midband frequency, this has little effect, but it could happen that, at some frequency, the feedback network produces positive instead of negative feedback. If this occurs, then self oscillation occurs at that frequency. For more information on this matter, reference can be made to Nyquist's criteria for stability and phase margins. These topics can be found in many textbooks under 'Amplifier Stability'.

Q23 *In the emitter follower circuit of Figure 11, the emitter resistor is 8200 Ω and the load resistor of 75 Ω is AC coupled to it. The silicon transistor has the following parameters:*

$$h_{FE} = 21, \qquad h_{fe} = 46, \qquad h_{ie} = 980\ \Omega.$$

At the frequency of operation, the capacitors can be assumed to have negligible reactance.

(*a*) *Calculate the emitter voltage under static conditions when the base current is 32 μA.*

(*b*) *Calculate the input signal required to produce a power dissipation of 200 mW in the load and the voltage swing at the output.*

(*c*) *Calculate the input impedance of the circuit.*

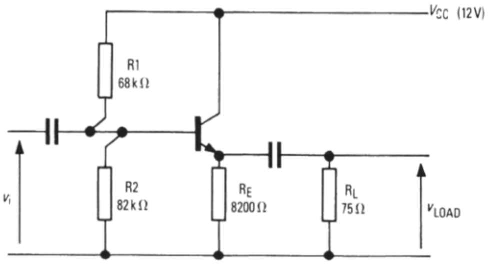


Figure 11

A23 (*a*) $I_C = h_{FE} I_B = 21 \times 32 \times 10^{-6}\ \text{A} = 0{\cdot}672\ \text{mA}.$

$$I_E = I_C + I_B = 0{\cdot}672 + 0{\cdot}032\ \text{mA} = 0{\cdot}704\ \text{mA}.$$

$$V_E = I_E R_E = 0{\cdot}704 \times 10^{-3} \times 8200\ \text{V} = \underline{5{\cdot}7728\ \text{V}.}$$

> Note that this value of V_E gives approximately half of V_{CC}, which is the condition for Class A operation. This value of V_E permits the emitter voltage to swing up towards 12 V, when the transistor approaches saturation and down towards 0 V as the transistor approaches cut-off.

(*b*) For a power dissipation of 200 mW in R_L,

$$P = \frac{V^2}{R_L}.$$

$$\therefore \qquad V_{LOAD} = \sqrt{(PR_L)}\ \text{volts},$$

$$= \sqrt{200 \times 10^{-3} \times 75},$$

$$= 3{\cdot}873\ \text{V}.$$

Under dynamic conditions (AC working), R_L is effectively in parallel with R_E so that the AC emitter load is given by

$$\frac{1}{R'_E} = \frac{1}{R_E} + \frac{1}{R_L},$$

$$= \frac{1}{8200} + \frac{1}{75}.$$

$$\therefore \quad R'_E = 74{\cdot}32\,\Omega.$$

For the emitter follower,

$$A_v = \frac{(1 + h_{fe})R'_E}{h_{ie} + (1 + h_{fe})R'_E},$$

$$= \frac{(1 + 46) \times 74{\cdot}32}{980 + (1 + 46) \times 74{\cdot}32},$$

$$= 0{\cdot}7809.$$

The output voltage is given by

$$v_O = v_{LOAD} = A_v v_i.$$

$$\therefore \quad v_i = \frac{v_{LOAD}}{A_v},$$

$$= \frac{3{\cdot}873}{0{\cdot}7809}$$

$$= \underline{4{\cdot}96\ \text{V}.}$$

The voltage swing at the output is the peak-to-peak value of the power-producing value (which is the RMS value).

$$\therefore \quad \text{voltage swing} = 2\sqrt{2}V_{LOAD},$$

$$= 2\sqrt{2} \times 3{\cdot}873\ \text{V},$$

$$= \underline{10{\cdot}954\ \text{V}.}$$

> The voltage swing at the emitter is less than V_{CC} and thus no distortion occurs. As the transistor moves towards cut-off, the emitter voltage falls from its static value to that value given by
>
> $$V_{E,STATIC} - \text{half the voltage swing},$$
>
> so that V_E falls to
>
> $$5{\cdot}7728 - \tfrac{1}{2}(10{\cdot}954) = 0{\cdot}2958\ \text{V}.$$
>
> As the base current is increased, the emitter voltage rises to a maximum value of
>
> $$V_{E,STATIC} + \text{half the voltage swing},$$
>
> so that V_E rises to
>
> $$5{\cdot}7728 + \tfrac{1}{2}(10{\cdot}954)\ \text{V} = 11{\cdot}2498\ \text{V},$$
>
> and the transistor is not driven to $V_{CE,SAT}$ which is some 0·2 V.

(*c*) The input impedance for the transistor is given by

$$Z_i = h_{ie} + (1 + h_{fe})R'_E,$$

$$= 980 + (1 + 46) \times 74{\cdot}32\,\Omega,$$

$$= 4473\,\Omega.$$

When the bias network is taken into account,

$$\frac{1}{Z_{\mathrm{i(CIRCUIT)}}}=\frac{1}{Z_{\mathrm{i}}}+\frac{1}{R_1}+\frac{1}{R_2},$$

$$=\frac{1}{4473}+\frac{1}{68000}+\frac{1}{82000}.$$

$$\therefore \quad Z_{\mathrm{i(CIRCUIT)}}=\underline{3993\,\Omega.}$$

This problem brings out one or two important aspects of the emitter-follower circuit. It is usually expected that the voltage gain will be very close to unity and that the input impedance will be very high. This is only the case when the effective load has a high value.

The input impedance can be increased considerably if, instead of using capacity coupling to the load resistor, transformer coupling is used. By using a step-down transformer, the reflected impedance into the primary would place a much higher ohmic value in parallel with R_{E} so that the effective value of R'_{E} would be much higher.

Q24 *An operational amplifier has an intrinsic gain of 80 dB and a corner frequency of 90 Hz. The roll-off characteristic of the operational amplifier is 20 dB/decade.*

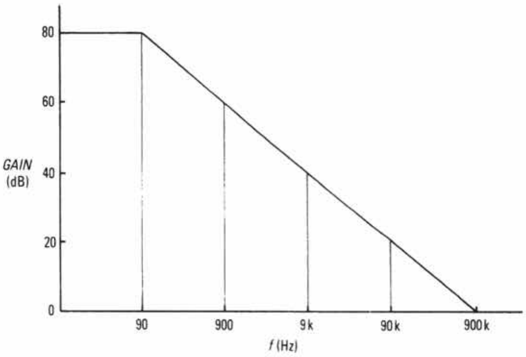
(*a*) *Sketch the response curve for the amplifier showing axes of decibels and frequency.*

(*b*) *Calculate the open-loop voltage gain of the op amp.*

(*c*) *When connected in the inverting mode, feedback is applied by using a feedback resistor of 180 kΩ, and an input resistor of 15 kΩ. Sketch the circuit arrangement and calculate the upper 3 dB frequency of the complete circuit.*

(*d*) *Calculate the gain in decibels of the complete circuit and sketch the new response curve.*

A24 (*a*)



The curve shown is known as the *piece-wise approximation*, where it is assumed that no loss occurs up to the corner frequency, after which the fall-off is 20 dB/decade. The largest error occurs at the corner frequency at which the practical gain is 3 dB down, that is 77 dB.

(*b*)

$$\mathrm{Gain}=20\log\frac{v_{\mathrm{o}}}{v_{\mathrm{i}}},$$

where v_{o} and v_{i} are the output and input voltages, respectively.

$$\therefore \quad \log\frac{v_{\mathrm{o}}}{v_{\mathrm{i}}}=\frac{\mathrm{gain}}{20}.$$

Taking antilogs,

$$v_{\mathrm{o}}:v_{\mathrm{i}}=10^{\mathrm{gain}/20}.$$

Therefore the open-loop voltage gain,

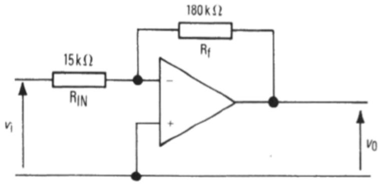
$$A_{\mathrm{v,OL}}=10^{\mathrm{gain}/20}.$$

Substituting values,

$$A_{v,OL} = 10^{80/20},$$

$$= \underline{10\,000.}$$

(*c*)



The closed-loop voltage gain,

$$A_v = -\frac{R_f}{R_{IN}} = -\frac{180\,000}{15\,000} = -12.$$

The new upper 3 dB frequency can be found by considering the gain-bandwidth product (GBP) which is assumed to be a constant for a given amplifier.

$$\text{GBP} = \text{midband voltage gain} \times \text{upper 3 dB frequency},$$

$$= 10\,000 \times 90\ \text{Hz} = 900\ \text{kHz}.$$

This value can also be obtained by reference to the response curve. When the gain is 0 dB (unit voltage gain) the curve cuts the frequency axis at 900 kHz.

Thus, when the midband voltage gain is reduced by feedback, since the gain bandwidth product is a constant.

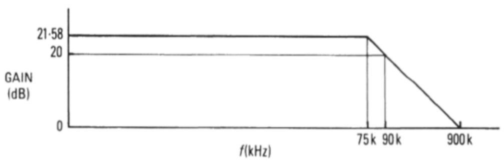
Upper 3 dB frequency

$$= \frac{\text{GBP}}{A_{v,CL}} = \frac{900 \times 10^3}{12}\ \text{Hz} = \underline{75\ \text{kHz.}}$$

(*d*) New gain $= 20 \log A_{v,CL}$ dB,

$= 20 \log 12$ dB,

$= \underline{21{\cdot}58\ \text{dB.}}$



Q25 *Figure 12 shows the circuit of an active integrator using an operational amplifier. The input signal is a sine wave of 6 V whose periodic time is 4 ms.*

(*a*) *Calculate the output voltage.*
(*b*) *Draw a diagram showing both the input and output waveforms indicating the voltage levels and time period.*

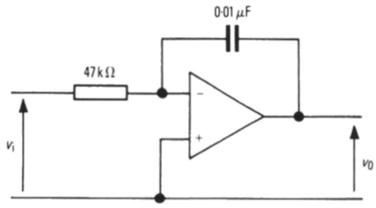


Figure 12

A25 (*a*) The input signal is given by

$$v = V \sin \omega t,$$

where $$V = 6\sqrt{2} \text{ volts, and}$$

$$\omega = 2\pi f = \frac{2\pi}{T} = \frac{2\pi}{4 \times 10^{-3}} = 500\pi \text{ rad/s.}$$

$$\therefore \quad v_i = 6\sqrt{2} \sin 500\pi t \text{ volts.}$$

For the active integrator,

$$v_o = -\frac{1}{CR}\int v_i \, dt,$$

$$= -\frac{1}{CR}\int V \sin \omega t \, dt,$$

$$= -\frac{V}{CR}\int \sin \omega t \, dt,$$

$$= -\frac{V}{CR}\left(\frac{-\cos \omega t}{\omega}\right),$$

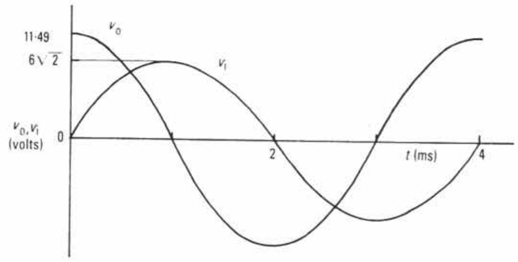
$$= \frac{V}{\omega CR} \cos \omega t.$$

Substituting values,

$$v_o = \frac{6\sqrt{2} \cos 500\pi t}{500\pi \times 0{\cdot}01 \times 10^{-6} \times 47 \times 10^3} \text{ volts,}$$

$$= \underline{11{\cdot}49 \cos 500\pi t \text{ volts.}}$$

(*b*)



Q26 An operational amplifier is connected as an active integrator whose feedback components have a time constant (τ) of 0·42 seconds.

The power supply to the circuit provides 12-0-12 volts, and saturation of the amplifier output occurs at 94% of V_{CC}. The voltage waveform shown in Figure 13 is applied to the input of the circuit.

(*a*) *Draw the circuit of the active integrator.*

(*b*) *If the resistive element is 220 kΩ, calculate the value of the other components included in the circuit.*

(*c*) *Obtain the equation of the input voltage.*

(*d*) *Calculate the period of time before the output voltage runs into saturation.*

(*e*) *Draw the output waveform for a period of 5 seconds after t = 0.*

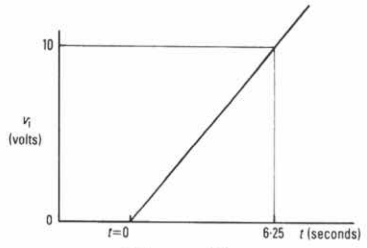
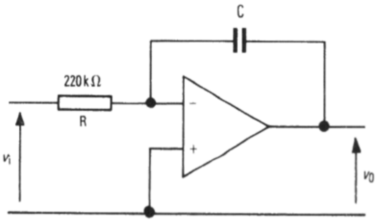


Figure 13

A26 (*a*)



(*b*)

$$\tau = CR \text{ seconds.}$$

$$\therefore \quad C = \frac{\tau}{R},$$

$$= \frac{0 \cdot 42}{220 \times 10^3} \text{ F},$$

$$= \underline{1 \cdot 91 \, \mu\text{F}.}$$

(*c*) Since the input voltage is a linear ramp, it has the form

$$y = mx + c,$$

where y is the input voltage, x is the time (t) and m is the gradient.

Also, when $t = 0$, $v_i = 0$. Therefore, $c = 0$.

$$\therefore \quad v_i = mt \text{ volts.}$$

The gradient is given by

$$m = \frac{10 - 0}{6 \cdot 25 - 0} = 1 \cdot 6 \text{ V/s.}$$

Thus the equation of the input voltage is

$$\underline{v_i = 1 \cdot 6t \text{ volts.}}$$

(*d*)

> Saturation occurs when the output voltage reaches 94% of V_{CC}. This time period can be found by obtaining the equation for the output voltage, after which the value of t can be calculated.

The output voltage of the active integrator is given by

$$v_o = -\frac{1}{CR} \int v_i \, dt,$$

and substituting values,

$$v_o = -\frac{1}{0 \cdot 42} \int 1 \cdot 6t \, dt,$$

$$= -\frac{1 \cdot 6}{0 \cdot 42} \int t \, dt,$$

$$= -3 \cdot 8095 \int t \, dt,$$

$$= -3 \cdot 8095 \left(\frac{t^2}{2} \right),$$

$$= -1 \cdot 905t^2 \text{ volts.}$$

Saturation occurs at 94% V_{CC}.

$$\therefore \quad V_{o,SAT} = 0 \cdot 94 \times 12,$$

$$= 11 \cdot 28 \text{ V.}$$

Rearranging the equation for t:

$$v_o = -1{\cdot}905t^2.$$

$$\therefore \quad t^2 = \frac{v_o}{-1{\cdot}905}.$$

$$\therefore \quad t = \sqrt{\left(\frac{v_o}{-1{\cdot}905}\right)} \text{ seconds.}$$

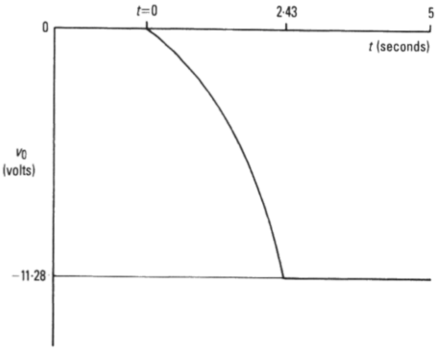
Note that the active integrator produces signal inversion, and therefore the positive ramp at the input produces negative saturation.

$$\therefore \quad t = \sqrt{\left(\frac{-11{\cdot}28}{-1{\cdot}905}\right)},$$

$$= 2{\cdot}43 \text{ seconds.}$$

So saturation occurs after 2·43 seconds.

(e)



The output voltage is of the form

$$v_o = kt^2,$$

which is of the form

$$y = mx^2,$$

which follows a square-law relationship, and, since m is negative, the output voltage is a negative going parabola until saturation is reached at $-11{\cdot}28$ V (when $t = 2{\cdot}43$ seconds).

Q27 The circuit of Figure 14 shows a free running multivibrator using discrete components. The frequency of operation is 200 kHz and the mark-space ratio 1 : 1. The transistors are silicon and have a static current gain of 34. The safe maximum collector current can be taken as 16 mA.

- (a) *Calculate values for R_L, R_B and C and suggest suitable preferred values.*
- (b) *Determine the rise time of the collector waveforms.*
- (c) *State whether the rise time is satisfactory and explain why.*

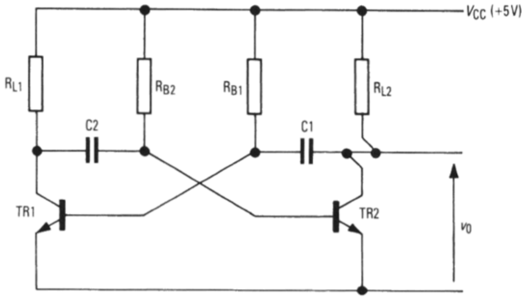


Figure 14

A27

Typical parameters for a silicon transistor are

$$V_{\mathrm{BE,SAT}} = 0{\cdot}8\ \mathrm{V} \qquad V_{\mathrm{CE,SAT}} = 0{\cdot}2\ \mathrm{V},$$

and these values should be used to calculate the values of the base and collector resistors. Having found a value for R_{B}, the value of the coupling capacitor can be obtained.

The collector load value is given by

$$R_{\mathrm{L}} = \frac{V_{\mathrm{CC}} - V_{\mathrm{CE,SAT}}}{I_{\mathrm{C}}},$$

$$= \frac{5 - 0{\cdot}2}{16 \times 10^{-3}},$$

$$= 300\ \Omega.$$

Similarly,

$$R_{\mathrm{B}} = \frac{V_{\mathrm{CC}} - V_{\mathrm{BE,SAT}}}{I_{\mathrm{B}}}, \qquad \text{and}$$

$$I_{\mathrm{B}} = \frac{I_{\mathrm{C}}}{h_{\mathrm{FE}}} = \frac{16 \times 10^{-3}}{34} = 0{\cdot}4706\ \mathrm{mA}.$$

$$\therefore \quad R_{\mathrm{B}} = \frac{5 - 0{\cdot}8}{0{\cdot}4706 \times 10^{-3}}\ \Omega = 8925\ \Omega$$

Since the safe maximum collector current is 16 mA, this value should not be exceeded and therefore the next higher preferred value should be used for R_{L}. In the case of R_{B}, if a higher value is used, the base current may not be sufficient to bottom the collector voltage, so the next lower preferred value should be used.

Use $R_{\mathrm{L}} = 330\ \Omega$ and $R_{\mathrm{B}} = 8200\ \Omega$.

For the free-running multivibrator of mark–space ratio 1:1, the frequency of operation is given by

$$f = \frac{1}{1{\cdot}386 C R_{\mathrm{B}}}\ \mathrm{Hz}.$$

$$\therefore \quad C = \frac{1}{1{\cdot}386 R_{\mathrm{B}} f}\ \mathrm{F}.$$

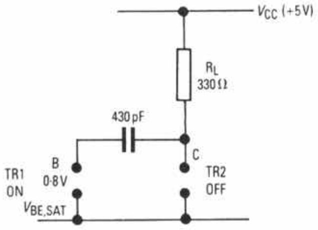
Substituting values,

$$C = \frac{1}{1{\cdot}386 \times 8200 \times 200 \times 10^{3}}\ \mathrm{F},$$

$$= 440\ \mathrm{pF}.$$

The closest preferred value of C is 430 pF, which produces a 2% increase in the frequency of operation.

(*b*) The rise time of the collector waveform is calculated by considering one of the quasi-stable states; for example when transistor TR1 is ON and TR2 OFF. The part of the circuit involved in the calculation is shown in the sketch.



The collector voltage of transistor TR2 rises towards $V_{CC}(+5\ \text{V})$ as the capacitor charges from V_{CC} via R_L and the base-emitter junction of TR1.

The rise time is given by

$$
\begin{aligned}
t_r &= 2{\cdot}2CR_L \text{ seconds,}\\
&= 2{\cdot}2 \times 430 \times 10^{-12} \times 330,\\
&= \underline{312\ \text{ns.}}
\end{aligned}
$$

(*c*)

To decide whether the rise time is satisfactory it must be compared with the duration of one half cycle of the collector waveform.

Since $T = \frac{1}{f}$, the duration of one half cycle is

$$
\begin{aligned}
\frac{T}{2} = \frac{1}{2f} &= \frac{1}{2 \times 200 \times 10^3} \text{ seconds,}\\
&= 2500\ \text{ns.}
\end{aligned}
$$

Comparing the rise time with the duration of one half cycle,

$$\frac{T/2}{t_r} = \frac{2500 \times 10^{-9}}{312 \times 10^{-9}}.$$

$$\therefore \qquad T/2 : t_r = 8:1.$$

This suggests that the rise time is a little slow because ideally it should be less than one tenth of the half cycle period in order to preserve the steep leading edge.

Q28 *The three stages of a cascade amplifier have voltage gains of 65, 73 and 42 when the inputs and outputs are correctly loaded with 500 Ω.*

(*a*) *Calculate the overall gain in decibels.*

(*b*) *What is the input voltage required to produce a peak load power of 12 W if the input signal is sinusoidal?*

A28 (*a*) Overall voltage gain

$$
\begin{aligned}
&= A_{v,1} \times A_{v,2} \times A_{v,3},\\
&= 65 \times 73 \times 42.
\end{aligned}
$$

$$\therefore \qquad A_{v,\text{TOTAL}} = 199\,290.$$

$$\text{Gain} = 20 \log 199\,290\ \text{dB}.$$

$$\therefore \qquad \text{Gain} = 106\ \text{dB}.$$

(*b*) For a sinusoidal input,

$$P = \frac{V_L^2}{R_L} \text{ watts,}$$

where V_L is the RMS value of the potential difference across the load resistor.

The peak power is given by

$$P_{\text{peak}} = \frac{(V_L\sqrt{2})^2}{R_L} = \frac{2V_L^2}{R_L} \text{ watts.}$$

Rearranging for the RMS voltage,

$$P_{\text{peak}} R_L = 2V_L^2.$$

$$\therefore \quad V_L = \sqrt{\left(\frac{P_{\text{peak}} R_L}{2}\right)}.$$

Substituting values,

$$V_L = \sqrt{\left(\frac{12 \times 500}{2}\right)},$$

$$= 54{\cdot}77 \text{ V}.$$

Since

$$v_o = A_{v,\text{TOTAL}} v_i,$$

$$v_i = \frac{v_o}{A_{v,\text{TOTAL}}},$$

$$= \frac{54{\cdot}77}{199\,290},$$

$$= \underline{0{\cdot}275 \text{ mV}.}$$

In an audio system, it is not sufficient for the speakers to be able to handle the average power which is given by using the RMS value of the voltage or current. The speakers must be capable of handling the peak power produced, without distortion, when the voltage or current sine wave passes through its maximum value, at which point the power is twice as great.

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